Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

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1. (Currently Amended) A method of fabricating a polysilicon emitter in a semiconductor transistor having an emitter window exposing a base region, the method comprising:

forming a first polysilicon layer within the emitter window on at least the base region;

forming an interfacial oxide layer in an upper portion of the first polysilicon layer; and

forming a second polysilicon layer on the interfacial oxide layer, wherein the second polysilicon layer is not in direct contact with the base region.

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2. (Original) The method of claim 1, wherein the emitter window is approximately .1 to .2 mm wide.

3. (Original) The method of claim 1, wherein the first polysilicon layer is formed to a thickness of approximately 30 to 100 Å.

4. (Original) The method of claim 3, wherein the interfacial oxide layer is formed by exposing oxygen to the first polysilicon layer and annealing.

5. (Original) The method of claim 3, wherein the interfacial oxide is formed to a thickness of approximately 5 to 50 Å.

6. (Original) The method of claim 5, wherein the second polysilicon layer is formed to a thickness of approximately 500 to 5000 Å excluding the depth of the emitter window.

7. (Original) The method of claim 1, wherein forming the second polysilicon layer comprises ion-implanting dopants into the second polysilicon layer.

8. (Original) The method of claim 1, further comprising annealing after forming the second polysilicon layer to diffuse dopants from the polysilicon emitter and into the base region.

9. (Currently Amended) A polysilicon emitter in a semiconductor transistor having an emitter window exposing a base region, comprising:

a first polysilicon layer within the emitter window on at least the exposed base region;

an interfacial oxide layer on the first polysilicon layer; and

a second polysilicon layer on the interfacial oxide, wherein the second polysilicon layer is not in direct contact with the base region.

10. (Original) The polysilicon emitter of claim 9, wherein the emitter window is approximately .1 to .2 mm wide.

11. (Original) The polysilicon emitter of claim 9, wherein the first polysilicon layer is less than approximately 100 Å thick.

12. (Original) The polysilicon emitter of claim 11, wherein the interfacial oxide is less than approximately 50 Å thick.

13. (Original) The polysilicon emitter of claim 12, wherein the second polysilicon layer is approximately 500 to 5000 Å thick excluding the depth of the emitter window.

14. (Currently Amended) A method of fabricating a bipolar transistor, comprising:

forming a collector region within a substrate;

forming a base region on the collector region;

forming an emitter dielectric layer on the base region;

forming an opening through the emitter dielectric layer to form an emitter window exposing a portion of the base region;

forming a first polysilicon layer within the emitter window on at least the exposed base region;

forming an interfacial oxide layer in an upper portion of the first polysilicon layer; and

forming a second polysilicon layer on the interfacial oxide, wherein the second polysilicon layer is not in direct contact with the base region.

15. (Original) The method of claim 14, wherein the emitter window is approximately .1 to .2 mm wide.

16. (Original) The method of claim 14, wherein the first polysilicon layer is formed to a thickness of approximately 30 to 100 Å.

17. (Original) The method of claim 16, wherein the interfacial oxide layer is formed by exposing oxygen to the first polysilicon layer and annealing.

18. (Original) The method of claim 16, wherein the interfacial oxide is formed to a thickness of approximately 5 to 50 Å.

19. (Original) The method of claim 17, wherein the second polysilicon layer is formed to a thickness of approximately 500 to 5000 Å excluding the depth of the emitter window.

20. (Original) The method of claim 14, wherein forming the second polysilicon layer comprises ion-implanting dopants into the second polysilicon layer.

21. (Original) The method of claim 14, further comprising annealing after forming the second polysilicon layer.

22. (Currently Amended) A bipolar transistor, comprising:

a substrate having a collector region;

a base region on the collector region;

an oxide layer on the base region, the oxide layer having an opening therethrough to form an emitter window exposing a portion of the base region;

a first polysilicon layer at least within the emitter window and on at least the exposed base region;

an interfacial oxide layer on the first polysilicon layer; and

a second polysilicon layer on the interfacial oxide, wherein the second polysilicon layer is not in direct contact with the base region.

23. (Original) The bipolar transistor of claim 22, wherein the emitter window is approximately .1 to .2 mm wide.

24. (Original) The bipolar transistor of claim 22, wherein the first polysilicon layer is less than approximately 100 Å thick.

25. (Original) The bipolar transistor of claim 24, wherein the interfacial oxide is less than approximately 50 Å thick.

26. (Original) The bipolar transistor of claim 25, wherein the second polysilicon layer is approximately 500 to 5000 Å thick excluding the depth of the emitter window.

27. (New) The method of claim 1, wherein the first polysilicon layer is in direct contact with an intrinsic base region.

28. (New) The method of claim 1, wherein the second polysilicon layer is not in direct contact with an intrinsic base region.

29. (New) The polysilicon emitter of claim 9, wherein the first polysilicon layer is in direct contact with an intrinsic base region.

30. (New) The polysilicon emitter of claim 9, wherein the second polysilicon layer is not in direct contact with an intrinsic base region.

31. (New) The method of claim 14, wherein the first polysilicon layer is in direct contact with an intrinsic base region.

32. (New) The method of claim 14, wherein the second polysilicon layer is not in direct contact with an intrinsic base region.

33. (New) The transistor of claim 22, wherein the first polysilicon layer is in direct contact with an intrinsic base region.

34. (New) The method of claim 22, wherein the second polysilicon layer is not in direct contact with an intrinsic base region.